App. No. 09/700,940
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REMARKS

New claim 7 is supported, for example, by page 5, lines 15-18 and page 6, lines 20-22.

Kinoshita (US 5,869,852) does not disclose or suggest a LSI layout method including first automatically laying out a plurality of logic gate cells, followed by calculation and placement of corresponding power supply capacitor cells, as required by claim 7. Rather, the reference teaches unit capacity cells (62) which are first arranged at all wiring channels (see column 15, lines 2-7).

The benefit of the layout method of claim 7 is silicon die space savings. According to the current invention, a power supply capacitor gate cell is only provided in space available after the initial layout of the logic gate cells.

Therefore, the current invention is unobvious of the cited references.

Respectfully submitted,

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